

Notice of References Cited	Application/Control No. 10/709,798		Applicant(s)/Patent Under Reexamination KARTSCHOKE ET AL.	
	Examiner Suchin Parihar		Art Unit 2825	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,378,109	04-2002	Young et al.	716/4
*	B	US-5,822,218	10-1998	Moosa et al.	716/4
*	C	US-2005/0007153	01-2005	Ding et al.	326/098
*	D	US-2004/0160239	08-2004	Reynick, Joseph A.	324/765
*	E	US-2002/0027391	03-2002	Hutamura et al.	307/130
*	F	US-2005/0218934	10-2005	Lee et al.	326/083
*	G	US-6,222,770	04-2001	Roohparvar, Frankie Fariborz	365/185.19
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	R. Rodriguez-Montanes, J.A. Segura, V.H. Champac, J. Figueras and J.A. Rubio, Current vs. logic testing of gate oxide short, floating gate and bridging failures in CMOS, Proc. Int. Test Conf., pp. 510-519, October 1991.
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.